These rejections of these claims are respectfully traversed insofar as these claims are amended. In response to this Office Action claim 22 has been cancelled and new claims 26-41 have been added. Accordingly, claims 23-41 are now pending.

Claims 23-25

Claims 23-25 stand allowable over the prior art of record.

Independent Claim 26

Claim 26 comprises a method for arranging bump pads on a surface of an integrated circuit die and includes the limitation of providing a first signal bump pad (601-604), connecting a first end of a first trace to the first signal bump pad, connecting a second end of the first trace to a first input/output cell (611) (see Figures 6-7). The first trace radiates in a first direction. In addition, claim 26 includes providing a second signal bump pad, connecting a first end of a second trace to the second signal bump pad (601-604), connecting a second end of the second trace to a second input/output cell (611). The second trace radiates in a second direction which is opposite the first direction. Claim 26 further includes disposing the first and second traces on opposite sides of a first line defined by the first signal bump and the second signal bump, providing a first power bump pad having a third trace radiating in the first direction and connecting to a first power bus (608, 609), providing a second power bump having a fourth trace radiating in the second direction and connecting to a second power bus (608, 609). The third and fourth trace are disposed on opposite sides of a second line defined by the first power bump and the second power bump.

Seefeldt et al. (U.S. Patent No. 4,978,633) discloses a gate array die with a variable size architecture. The array of circuit devices includes gate supercells (31) and input/output supercells (32) (see Figure 2). Each of the input/output supercells contains an arrangement of adjacent I/O cells (61-65) (see Figure 3). Each I/O cell contains signal bump pads in the form of an input terminal pad (131) and an output terminal pad (132). In addition to the I/O cells, each input/output supercell contains a pair of power bus regions (51, 52) along opposite sides of the arrangement of I/O cells. The power bus regions each contain a pad (71, 75).

Seefeldt does not disclose or suggest providing traces which connect the signal bump pads to the input/output cells. In Seefeldt, the signal bump pads are formed directly on the input/output cells, and as a result, traces are not required to connect the signal bump pads to the input/out cells. The traces disclosed in Seefeldt are used to connect the signal bump pads to non-input/output cell components (see specification, column 4, lines 37-40: "[t]hrough input terminal pad 131, input cell 631 receives input signals from the outside world and couples those signals through driver 91 and over line 92 to an interconnected global routing channel..."; and see specification, column 4, lines 48-52: "[l]inks 102 and 103 extend to the right-hand edge portion of the output cell 630 for interconnecting to a global routing channel adjacent the right-hand edge of the input/output supercell shown in FIG. 3."). In addition, the first and second traces in Seefeldt do not radiate in opposite directions. Thus, it is respectfully submitted that claim 26 is in condition for allowance.

Dependent Claims 27-30

Dependent claims 27-30 depend from claim 26 and are similarly patentable. It is respectfully submitted that these claims are in condition for allowance.

Independent Claim 31

Claim 31 comprises a method for distributing connecting pads on a surface of a semiconductor die by calculating a power-signal ratio, establishing a number N of I/O bump pads to be allocated per pair of power bump pads based on the power-signal ratio, arranging the N I/O bump pads and pair of power bump pads linearly and repeating the linear arrangement within four edge groups on the surface of the die, identifying four corner regions, and arranging a core power group within the center of the edge groups and the corner regions (see specification, page 7, lines 14-32).

Applicant respectfully contends that Seefeldt teaches away from arranging the input/output bump pads and power bump pads linearly. In Seefeldt, the adjacent input/output cells have their pads offset from one another (see Figure 3). The purpose of this offset is to facilitate tab-bonding to the pads (primarily to prevent misbonding from the carrier interconnect leads for

adjacent input/output cells) (see column 4, lines 53-58). Thus, it is respectfully submitted that claim 31 is in condition for allowance.

Dependent Claims 32-35

Dependent claims 32-35 depend from claim 31 and are similarly patentable. Claim 32 includes the additional limitation that the N I/O bump pads and pair of power bump pads are arranged in a column (see specification, page 7, line 22). Seefeldt discloses a non-column arrangement where the I/O bump pads and power bump pads are offset. Claim 33 includes additional limitations similar to allowable claim 23. Claim 34 includes the additional limitation of designating two bump pads (305, 306) in each sector closest to an edge of the die as power bump pads (see Figure 3 and specification, page 8, lines 2-5). Seefeldt does not teach or suggest positioning two power bump pads closest to an edge of the die. Seefeldt discloses positioning a pair of power bus regions (51, 52) along opposite edges of the input/output cells (see Figure 3 and specification, column 4, lines 27-31: ".. each input/output supercell contains a pair of power bus region 51 and 52 along opposite edges of the arrangement of input/output cells 61-64."). It is respectfully submitted that these claims are in condition for allowance.

Independent claim 36

For the same reasons discussed above in regards to claim 26, it is respectfully submitted that claim 36 is in condition for allowance.

Dependent Claims 37-40

Dependent claims 37-40 depend from claim 36 and are similarly patentable. It is respectfully submitted that these claims are in condition for allowance.

Independent Claim 41

Claim 41 comprises a method for arranging bump pads on a surface of a flip-chip die by providing at least one power bump, linearly aligning a plurality of input/output bumps, wherein the

linearly aligned plurality of input/output bumps are aligned with at least one power bump. Claim 41 further includes the limitation of positioning at least one power bump intermediate among the linearly aligned plurality of input/output bumps (see Figures 6-7 and specification, page 14, lines 23-25).

As discussed above in regards to claim 31, Seefeldt teaches away from linearly aligning the input/output bumps and power bumps. In addition, Seefeldt does not disclose or suggest positioning at least one power bump intermediate among a plurality of input/output bumps. Seefeldt, on the other hand, discloses positioning a pair of power bus regions along opposite edges of the input/output cells (see Figure 3 and specification, page 8, lines 2-5). Thus, it is respectfully submitted that claim 41 is in condition for allowance.

Concluding Remarks

Accordingly, issuance of the Notice of Allowance at an early date is in order and is respectfully requested. If there are any remaining issues, the Examiner is encouraged to telephone counsel to seek to resolve them.

Respectfully submitted,

Dated: September 15, 1998

Douglas N. Larson
Registration No. 29,401

OPPENHEIMER WOLFF & DONNELLY LLP
2029 Century Park East, 38th Floor
Los Angeles, California 90067
Telephone: (310) 788-5000
Facsimile: (310) 377-1297